REMARKS

1. Claims 2, 3, 5-14 and 17-19 remain pending in the application, and Claims 20-23 have been withdrawn as subject to a restriction. The present Office Action rejects Claims 2-3, 5-7, 13-14, and 17 under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 2, 7-14 and 17-19 are rejected as anticipated under 35 U.S.C. § 102(b). Claims 3, 5, and 6 are rejected as unpatentable under 35 U.S.C. § 103(a).

2. Claims 2-3, 5-7, 13-14, and 17 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter Applicant regards as the invention. The rejection states that Claim 2 is indefinite because the phrase, "a control input . . . all available power supply voltage" is indefinite because it is misdescriptive. The Examiner has asked Applicant to show that the claim meets the requirements of under 35 U.S.C. § 112, second paragraph.

By minimizing the number of components in the circuit, each delay cell causes the least parasitic capacitance and voltage drop possible. As explained in pp. 5 and 6 of the specification, and with reference to Fig. 3a of the application, positive feedback amplifier 50 is connected so that transistors 56, 58 act as pull-up transistors, while the transistors in the linear amplifier 52 act as pull-down transistors. Specification, p. 5, lines 26-28. The circuit is power by the voltage (difference in potential), V_{pos} -V_{neg}. These supply voltages represent the maximum voltage and the minimum voltage available to the circuit. The voltage V_{pos} -V_{neg} represents the maximum available voltage difference or voltage swing available in the circuit.

Thus, the delay unit is fully differential, with the positive feedback portion 50 coupling the outputs of the linear amplifier 52. The circuit works by forcing both outputs of the delay stage to have 180 degrees of phase difference. Thus, there is a large voltage swing from nearly the voltage of the negative voltage source to the voltage of the positive voltage source. Specification, p. 6, lines 1-5. In this manner, the cell can be said to be able to use nearly all the available voltage, and thus to have a larger range of delay outputs for the user of the cell.

In response to the rejection for indefiniteness, Applicants have also amended the specification and claims to make it clear that the Vpos "input and control voltage" is more clearly stated as the supply voltage or the power supply voltage. Support for the amendments to Claims 2, 3, 5, 7, and 13, and for the amendments to the specification, is found at least in the specification at p. 3, lines 25-26, stating that a control input voltage, also acting as a positive power supply, is connected to the drains of the transistors.

3. Claims 2, 7-14, and 17-19 are rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Pat. No. 5,568,099 to He Du ("Du"). The rejection cites Figs. 11 and 15 of Du, and states that Du shows all the components of these claims. Applicants traverse the rejections.

Claim 2

Fig. 15 of Du, and the accompany text, shows a clipper transistor 4950 connected across the outputs of the amplifier, the clipper transistor turning on whenever the positive output po-1 connected to its drain or the negative output no-1 connected to its source becomes less than the difference between the bias voltage V_{clp} and a threshold voltage V_{th} of the clipper transistor. Du, col. 8, lines 48-55. The advantage stated by Du for the clipper transistor is that it replaces the diodes that were formerly used, and thus increases the frequency response of the resulting VCO shown in Du's Fig. 11. Du, col. 8, lines 58-67. This prior art corresponds to the prior art depicted in Fig. 1 of the application, in which load transistors 12 are connected as diodes with their gates connected to their drains. Application, Fig. 1 and text at p. 1, lines 22-27.

Thus, Du describes a circuit which functions in a manner opposite from the claimed invention, with a different and opposed goal: Du seeks to limit the voltage swings of the amplifiers for a better frequency response, while embodiments of the present invention seek to use "all available power supply voltage," as recited in the claim, or "headroom" available. See present specification, p. 6, lines 1-4. In addition, Du requires elements that are not present in the claims, including the "clipper" transistor and its voltage source. Thus, Du does not describe a four-transistor differential

controlled delay unit, or two of them in series, as required by Claim 2. Applicant submits that the rejection is overcome.

Claims 7-14 and 17-19

Claim 7 recites a voltage controlled oscillator comprising two four-transistor delay units in series. As discussed above with reference to Fig. 2, Du does not teach the four-transistor delay unit of the present application. Accordingly, Du does not anticipate Claim 7. Claims 8-12 depend from Claim 7 and are allowable for the same reason. Claim 13 depends from Claim 7, and Claims 14, and 17-19 depend from Claim 7 or Claim 13, and are allowable at least because Claim 7 is also allowable.

4. Claims 3, 5, and 6 are rejected under 35 U.S.C. § 103(a) as unpatentable in view of U.S. Pat. No. 5,568,099 to He Du ("Du") and further in view of U.S. Pat. No. 5,994,939 to Luke Johnson et al. ("Johnson"). The rejection states that Du discloses all the limitations of Claim 3 except for the fifth and sixth transistors, and that Johnson discloses the fifth and sixth transistors in Fig. 4. Applicant traverses the rejection on the grounds that the combination does not suggest all the limitations of Claim 3, and on the grounds that the combination of Johnson and Du is improper.

The combination does not suggest the claimed invention

Fig. 4 of Johnson is described as a single-unit delay cell. Johnson, col. 3, lines 7-8. The embodiment of Fig. 4 is clearly described as including an active side 70, an inactive side, 80, and a current steering circuit 60. The figure depicts inputs, INZ and IN, and outputs, OUT and OUTZ. The delay cell of Johnson comprises eighteen transistors, in addition to load capacitors (not shown in the figure) for proper performance of the active portion 70. Johnson, col. 4, lines 17-19. Johnson does not merely teach that two transistors are used in parallel in order to reduce the load resistance of the circuit, Johnson teaches a far more complicated circuit, with an active side and a passive side, and a current regulating circuit, to control the amount of current flowing in the active side. Johnson teaches that current is shunted to the inactive side

80 by steering circuit 60 in order to increase the frequency response of the cell. Johnson, col. 4, lines 8-19. As noted above in the discussion of Claim 2, Du uses a clipper transistor to limit the applied voltages and to improve frequency response.

Thus, a fair combination of Du and Johnson would be to replace the clipper transistor of Du with not merely a doubling of the input transistors, but also with the addition of an inactive side and a current regulating circuit. Accordingly, the combination of Du and Johnson does not suggest the limitations of Claim 3, but rather a far more complicated circuit, with perhaps as many as 18 transistors.

The combination of Du and Johnson is improper

As noted above, Du achieves increased speed or frequency response through the use of a clipper transistor. Without benefit of the present application, there is no motivation to take one very small portion of Johnson, the use of two transistors in parallel, and apply this very limited portion to Du, in order to increase frequency response. Accordingly, there is insufficient motivation to combine Du and Johnson, and the rejection is improper for this reason.

Claim 3 is thus allowable, and Claims 5 and 6 are allowable at least because Claim 3 is allowable. In addition, Du does not teach or suggest all the limitations of Claims 5 and 6, at least because Du uses a clipper transistor to increase frequency response, whereas the claims recite a configuration of the transistors themselves (ratio of width to length) to achieve a very high frequency response. Accordingly, Du does not teach or suggest all the limitations of Claims 3, 5 and 6, and the rejections are overcome.

5. Applicant respectfully requests the Examiner to withdraw the rejections and to advance the Application to allowance.

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